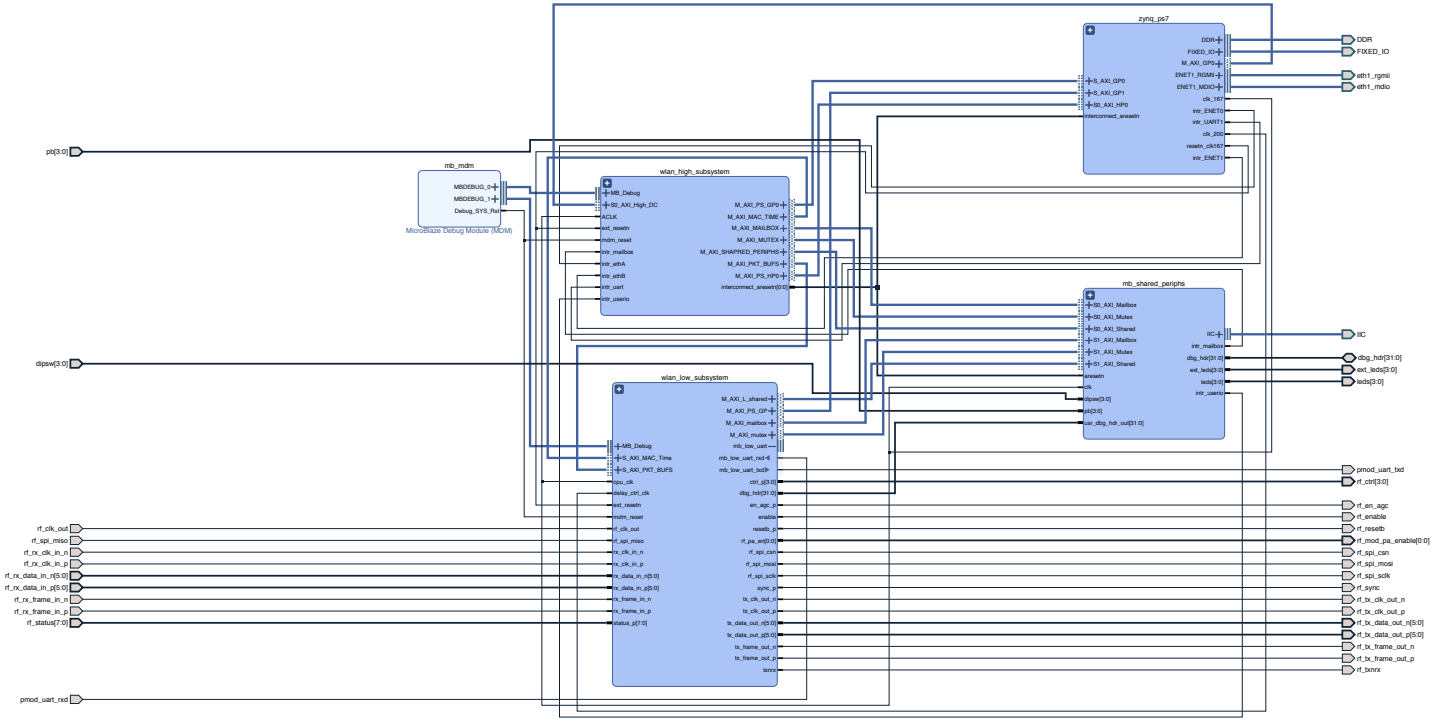
zynq_ps7
DDR
FIXED_IO
M_AXI_GP0
ENET1_RGMII
ENET1_MDIO
clk_167
intr_ENET0
intr_UART1
clk_200
resetn_clk167
intr_ENET1
S_AXI_GP0
S_AXI_GP1
S0_AXI_HP0
interconnect_aresetn
DDR
FIXED_IO
eth1_rgmii
eth1_mdio
pb[3:0]
mb_mdm
MBDEBUG_0
MBDEBUG_1
Debug_SYS_Rst
MicroBlaze Debug Module (MDM)
wlan_high_subsystem
MB_Debug
S0_AXI_High_DC
ACLK
ext_resetn
mdm_reset
intr_mailbox
intr_ethA
intr_ethB
intr_uart
intr_userio
M_AXI_PS_GP0
M_AXI_MAC_TIME
M_AXI_MAILBOX
M_AXI_MUTEX
M_AXI_SHAPRIED_PERIPHS
M_AXI_PKT_BUFS
M_AXI_PS_HP0
interconnect_aresetn[0:0]
mb_shared_periphs
S0_AXI_Mailbox
S0_AXI_Mutex
S0_AXI_Shared
S1_AXI_Mailbox
S1_AXI_Mutex
S1_AXI_Shared
aresetn
clk
dipsw[3:0]
pb[3:0]
sar_dbg_hdr_out[31:0]
IIC
intr_mailbox
dbg_hdr[31:0]
ext_leds[3:0]
leds[3:0]
intr_userio
IIC
dbg_hdr[31:0]
ext_leds[3:0]
leds[3:0]
dipsw[3:0]
wlan_low_subsystem
M_AXI_L_shared
M_AXI_PS_GP
M_AXI_mailbox
M_AXI_mutex
MB_Debug
S_AXI_MAC_Time
S_AXI_PKT_BUFS
mac_clk
delay_ctrl_clk
ext_resetn
mdm_reset
rf_clk_out
rf_spi_miso
rx_clk_in_n
rx_clk_in_p
rx_data_in_n[5:0]
rx_data_in_p[5:0]
rx_frame_in_n
rx_frame_in_p
status_p[7:0]
mb_low_uart
mb_low_uart_rxd
mb_low_uart_txd
ctrl_p[3:0]
dbg_hdr[31:0]
en_agc_p
enable
resetb_p
rf_pa_en[0:0]
rf_spi_csn
rf_spi_mosi
rf_spi_sclk
sync_p
tx_clk_out_n
tx_clk_out_p
tx_data_out_n[5:0]
tx_data_out_p[5:0]
tx_frame_out_n
tx_frame_out_p
txnrx
pmod_uart_txd
rf_ctrl[3:0]
rf_clk_out
rf_spi_miso
rf_rx_clk_in_n
rf_rx_clk_in_p
rf_rx_data_in_n[5:0]
rf_rx_data_in_p[5:0]
rf_rx_frame_in_n
rf_rx_frame_in_p
rf_status[7:0]
pmod_uart_rxd
rf_en_agc
rf_enable
rf_resetb
rf_mod_pa_enable[0:0]
rf_spi_csn
rf_spi_mosi
rf_spi_sclk
rf_sync
rf_tx_clk_out_n
rf_tx_clk_out_p
rf_tx_data_out_n[5:0]
rf_tx_data_out_p[5:0]
rf_tx_frame_out_n
rf_tx_frame_out_p
rf_txnrx